Very Low Noise, High Accuracy, Quad Universal Filter Building Block

FEATURES

- **Four Identical 2nd Order Filters in an SSOP Package**
- **Center Frequency Error: ≤±0.3% Typ**
- **Low Noise: ≤40μV_{RMS} per 2nd Order Section, Q ≤ 5**
- **High Dynamic Range: THD + Noise ≤0.01%**
- Low DC Offsets: ≤10mV Typ per 2nd Order Section
- Clock-to-Center Frequency Ratio: 100:1
- No Aliasing for Input Frequencies up to 200 × f_{CUTOFF}
- Maximum Center Frequency up to 56kHz (V_S = ±5V)
- Operates from ±1.57V to ±5V Power Supplies

APPLICATIONS

- Linear Phase Bandpass Filters
- Dual 4th Order Phase Matched Filters
- High Selectivity Bandpass Filters
- Notch Filters
- Audio Equalizer Filters
- Noise Cancellation Filters

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DESCRIPTION

The LTC®1068 consists of four identical, low noise, high accuracy 2nd order switched-capacitor filter building blocks. Each building block, together with three to five resistors, can provide 2nd order filter functions like lowpass, bandpass, highpass and notch. High precision, high performance, quad 2nd order, dual 4th order or 8th order filters can also be designed with an LTC1068. The center frequency of each 2nd order section is tuned by an external clock. The clock-to-center frequency ratio is internally set to 100:1 and can be modified by external resistors.

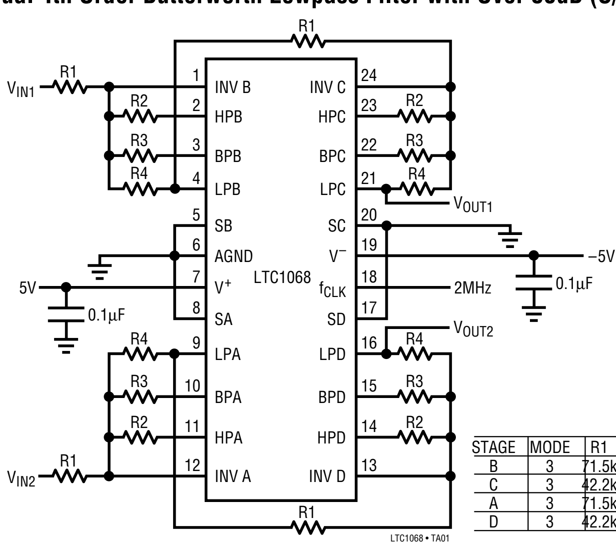
The sampling rate of the LTC1068 is twice the clock frequency. The maximum input frequency can approach twice the clock frequency before aliasing occurs.

A customized version of the LTC1068 in a 16-lead SO with internal thin film resistors can be obtained. Clock-to-center frequency ratios higher or lower than 100:1 can also be obtained. Please contact LTC Marketing for details.

The LTC1068 is available in a 24-pin PDIP and 28-pin SSOP surface mounted package.

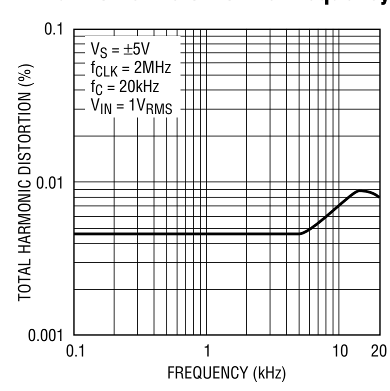
TYPICAL APPLICATION

20kHz, Dual 4th Order Butterworth Lowpass Filter with Over 80dB (S/N + THD)



STAGE	MODE	R1	R2	R3	R4
B	3	71.5k	40.2k	49.9k	40.2k
C	3	42.2k	75.0k	40.2k	75.0k
A	3	71.5k	40.2k	49.9k	40.2k
D	3	42.2k	75.0k	40.2k	75.0k

Harmonic Distortion vs Frequency



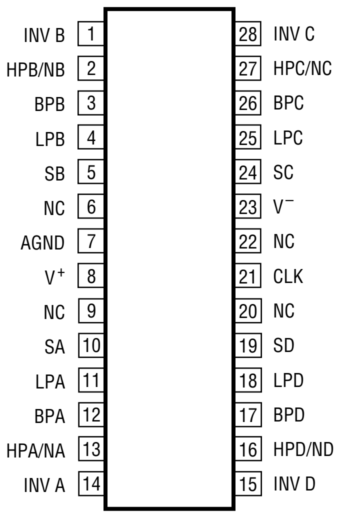
ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V^+ to V^-) 12V
Power Dissipation 500mW
Input Voltage at Any Pin .... $V^- - 0.3V \leq V_{IN} \leq V^+ + 0.3V$

Operating Temperature Range
LTC1068C .... 0°C to 70°C
LTC1068I .... –40°C to 85°C
Storage Temperature Range .... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) .... 300°C

PACKAGE/ORDER INFORMATION

TOP VIEW

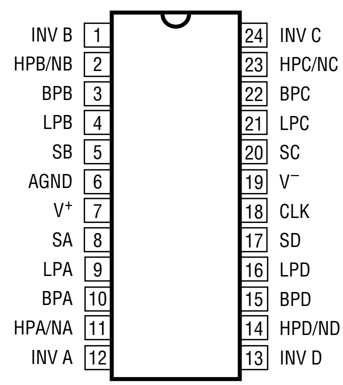


G PACKAGE
28-LEAD PLASTIC SSOP
$T_{JMAX} = 110°C$, $\theta_{JA} = 95°C/W$

ORDER PART NUMBER

LTC1068CG
LTC1068IG

TOP VIEW



N PACKAGE
24-LEAD PDIP
$T_{JMAX} = 110°C$, $\theta_{JA} = 65°C/W$

ORDER PART NUMBER

LTC1068CN
LTC1068IN

Consult factory for Military grade parts.

ELECTRICAL CHARACTERISTICS (Internal Op Amps) $V_S = \pm5V$, $T_A = 25°C$, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Operating Supply Voltage Range			±1.57		±5.5	V
Voltage Swings	$V_S = \pm1.57V$, $R_L = 5k$	●	±0.65	±0.9		V
	$V_S = \pm2.375V$, $R_L = 5k$	●	±1.50	±1.7		V
	$V_S = \pm5V$, $R_L = 5k$	●	±3.60	±4.3		V
Output Short-Circuit Current (Source/Sink)	$V_S = \pm2.375V$			17/6		mA
	$V_S = \pm5V$			20/15		mA
DC Open-Loop Gain	$R_L = 5k$			85		dB
GBW Product				6		MHz
Slew Rate				10		V/µs

ELECTRICAL CHARACTERISTICS (Complete Filter) $V_S = \pm5V$, $T_A = 25°V$, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Center Frequency Range, f_O (Note 1)				0.1 to 50		kHz
Input Frequency Range				0 to 1		MHz
Clock-to-Center Frequency, f_{CLK}/f_O	$V_S = \pm2.375V$, $f_{CLK} = 1MHz$, Mode 1, $f_O = 10kHz$, Q = 5, R1 = R3 = 49.9k, R2 = 10k	 ●		100 ±0.3	100 ±0.8 100 ±0.9	% %
	$V_S = \pm5V$, $f_{CLK} = 1MHz$, Mode 1, $f_O = 10kHz$, Q = 5, R1 = R3 = 49.9k, R2 = 10K	 ●		100 ±0.3	100 ±0.8 100 ±0.9	% %
Clock-to-Center Frequency Ratio, Side-to-Side Matching (Note 2)	$V_S = \pm2.375V$, $f_{CLK} = 1MHz$, Q = 5 $V_S = \pm5V$, $f_{CLK} = 1MHz$, Q = 5	● ●		±0.25 ±0.25	±0.9 ±0.9	% %
Q Accuracy (Note 2)	$V_S = \pm2.375V$, $f_{CLK} = 1MHz$, Q = 5 $V_S = \pm5V$, $f_{CLK} = 1MHz$, Q = 5	● ●		±1 ±1	±3 ±3	% %
f_O Temperature Coefficient				±1		ppm/°C
Q Temperature Coefficient				±5		ppm/°C
DC Offset Voltage (Note 2) (See Table 1)	$V_S = \pm5V$, $f_{CLK} = 1MHz$, V_{OS1} (DC Offset of Input Inverter) $V_S = \pm5V$, $f_{CLK} = 1MHz$, V_{OS2} (DC Offset of First Integrator) $V_S = \pm5V$, $f_{CLK} = 1MHz$, V_{OS3} (DC Offset of Second Integrator)	 ● ● ●		 0 −2 −5	 ±15 ±25 ±40	 mV mV mV
Clock Feedthrough				0.1		mV_{RMS}
Max Clock Frequency	$V_S = \pm5V$, $Q \le 2.0$, Mode 1			5.6		MHz
Power Supply Current	$V_S = \pm1.57V$, $f_{CLK} = 1MHz$ $V_S = \pm2.375V$, $f_{CLK} = 1MHz$ $V_S = \pm5V$, $f_{CLK} = 1MHz$			2.0 5.0 7.5	3.75 7.50 11.0	mA mA mA
	$V_S = \pm1.57V$, $f_{CLK} = 1MHz$ $V_S = \pm2.375V$, $f_{CLK} = 1MHz$ $V_S = \pm5V$, $f_{CLK} = 1MHz$	● ● ●		2.5 5.5 8.0	4.5 8.5 12.0	mA mA mA

The ● denotes specifications which apply over the full operating temperature range.

Note 1: See performance characteristics.

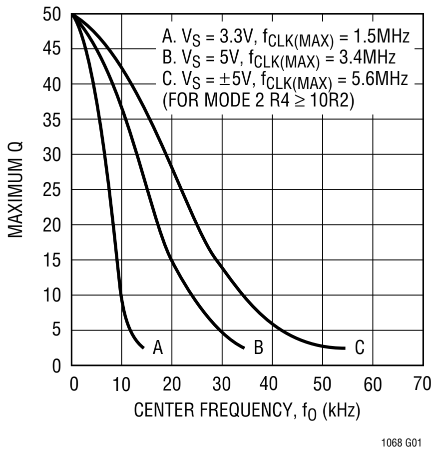
Note 2: Side D is guaranteed by design.

Table 1. Output DC Offsets One 2nd Order Section

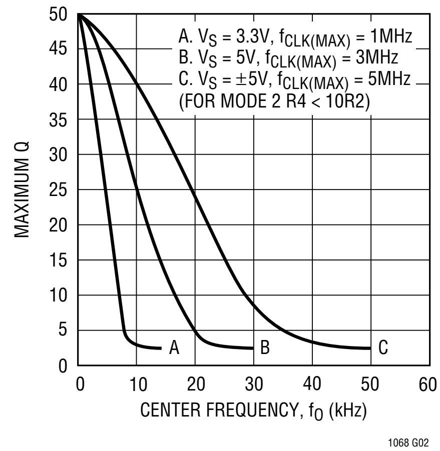
MODE	V_{OSN}	V_{OSBP}	V_{OSLP}
1	$V_{OS1}[(1/Q) + 1 + \|HOLP\|] - V_{OS3}/Q$	V_{OS3}	$V_{OSN} - V_{OS2}$
1b	$V_{OS1}[(1/Q) + 1 + R2/R1] - V_{OS3}/Q$	V_{OS3}	$\sim(V_{OSN} - V_{OS2})(1 + R5/R6)$
2	$[V_{OS1}(1 + R2/R1 + R2/R3 + R2/R4) - V_{OS3}(R2/R3)X$ $[R4/(R2 + R4)] + V_{OS2}[R2/(R2 + R4)]$	V_{OS3}	$V_{OSN} - V_{OS2}$
3	$V_{OS2} = V_{OS(HP)}$	V_{OS3}	$V_{OS1}[1 + R4/R1 + R4/R2 + R4/R3] - V_{OS2}(R4/R2) - V_{OS3}(R4/R3)$

TYPICAL PERFORMANCE CHARACTERISTICS

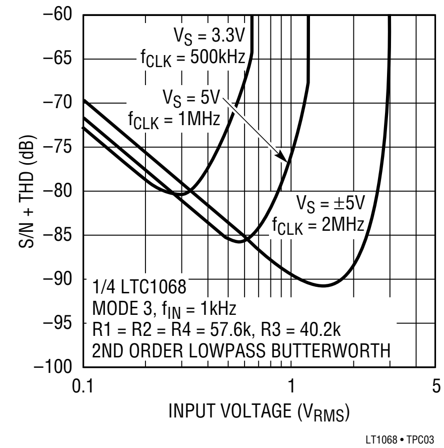
Maximum Q vs Center Frequency (Modes 1, 1B, 2)



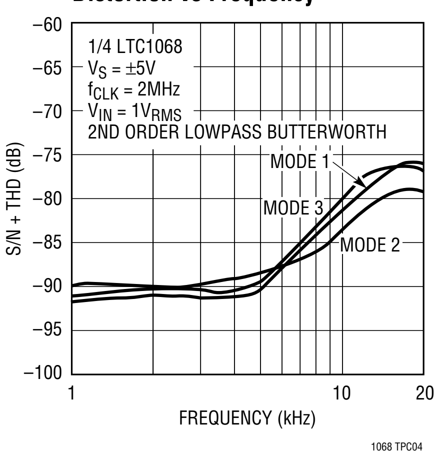
Maximum Q vs Center Frequency (Modes 2, 3)



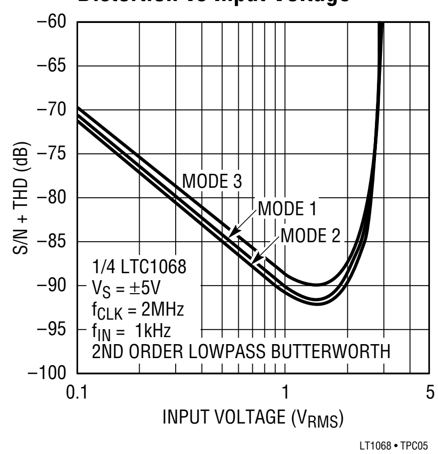
Signal to Noise + Total Harmonic Distortion vs Input Voltage



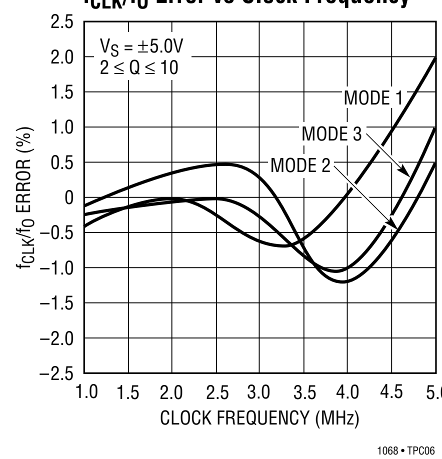
Signal to Noise + Total Harmonic Distortion vs Frequency



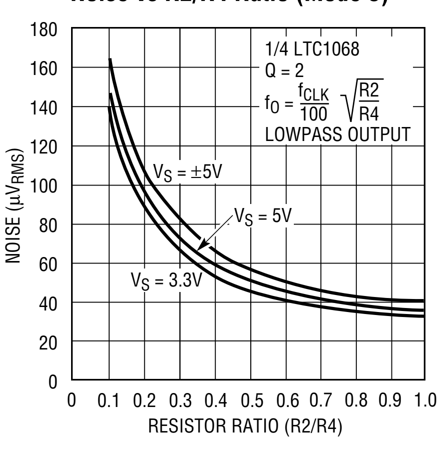
Signal to Noise + Total Harmonic Distortion vs Input Voltage



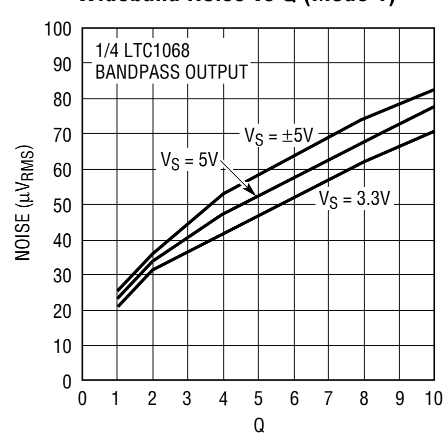
f_{CLK}/f_O Error vs Clock Frequency



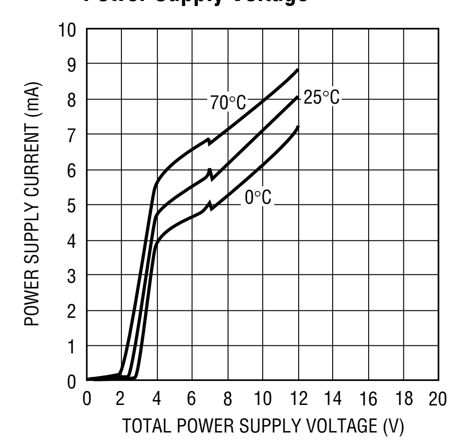
Noise vs R2/R4 Ratio (Mode 3)



Wideband Noise vs Q (Mode 1)



Power Supply Current vs Power Supply Voltage



PIN FUNCTIONS

Power Supply Pins

The V^+ and V^- pins should each be bypassed with a 0.1μF capacitor to an adequate analog ground. The filter's power supplies should be isolated from other digital or high voltage analog supplies. A low noise linear supply is recommended. Using a switching power supply will lower the signal-to-noise ratio of the filter. Figures 1 and 2 show typical connections for dual and single supply operation.

Analog Ground Pin

The filter's performance depends on the quality of the analog signal ground. For either dual or single supply operation, an analog ground plane surrounding the package is recommended. The analog ground plane should be connected to any digital ground at a single point. For single supply operation, AGND should be bypassed to the analog ground plane with at least a 0.47μF capacitor (Figure 2).

Two internal 10k resistors bias the analog ground pin to one half the power supply voltage across the IC. For instance, if the LTC1068 operates with a single 5V supply, the potential of the analog ground pin is 2.5V ±0.5%

Clock Input Pin

Any TTL or CMOS clock source with a square-wave output and 50% duty cycle (±10%) is an adequate clock source for the device. The power supply for the clock source should not be the filter's power supply. The analog ground for the filter should be connected to clock's ground at a single point only. Table 2 shows the clock's low and high level threshold values for dual or single supply operation.

Table 2. Clock Source High and Low Threshold Levels

POWER SUPPLY	HIGH LEVEL	LOW LEVEL
Dual Supply = ±5V	≥ 1.53V	≤ 0.53V
Single Supply = 5V	≥ 1.53V	≤ 0.53V
Single Supply = 3.3V	≥ 1.20V	≤ 0.53V

A pulse generator can be used as a clock source provided the high level ON time is greater than 0.2μs. Sine waves are not recommended for clock input frequencies less than 100kHz, since excessively slow clock rise or fall times generate internal clock jitter (maximum clock rise or fall time ≤ 1μs). The clock signal should be routed from the right side of the IC package and perpendicular to it to avoid coupling to any input or output analog signal path. A 200Ω

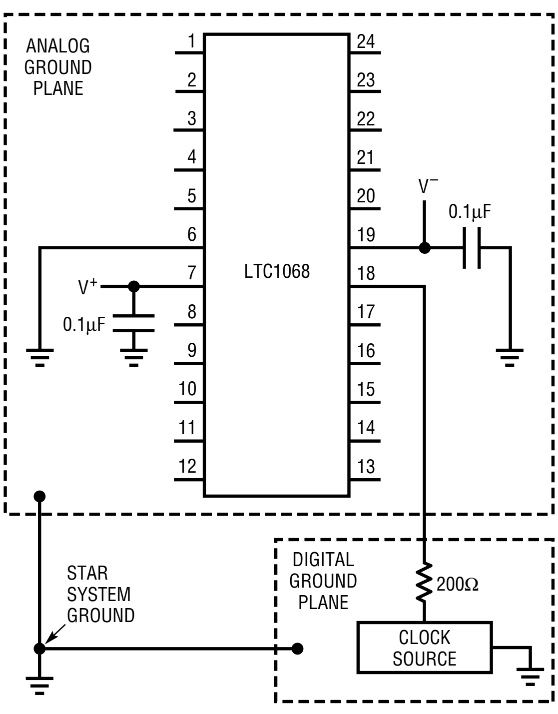


Figure 1. Dual Supply Ground Plane Connections

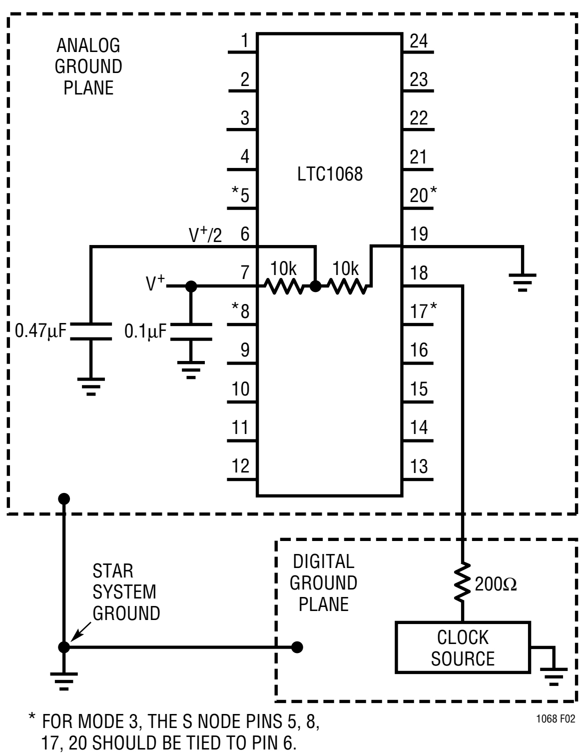


Figure 2. Single Supply Ground Plane Connections

PIN FUNCTIONS

resistor between clock source and Pin 11 will slow down the rise and fall times of the clock to further reduce charge coupling (Figures 1 and 2).

Output Pins

Each 2nd order section of the LTC1068 has three outputs that typically source 17mA and sink 6mA. Driving coaxial cables or resistive loads less than 20k will degrade the total harmonic distortion performance of any filter design. When evaluating the distortion or noise performance of a particular filter design implemented with LTC1068, the final output of the filter should be buffered with a wideband, noninverting high slew rate amplifier (Figure 3).

Inverting Input Pins

These pins are the inverting inputs of internal op amps and are susceptible to stray capacitive coupling from low impedance signal outputs and power supply lines.

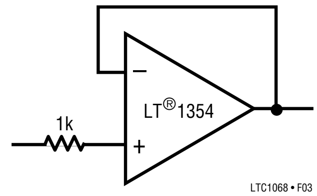


Figure 3. Wideband Buffer

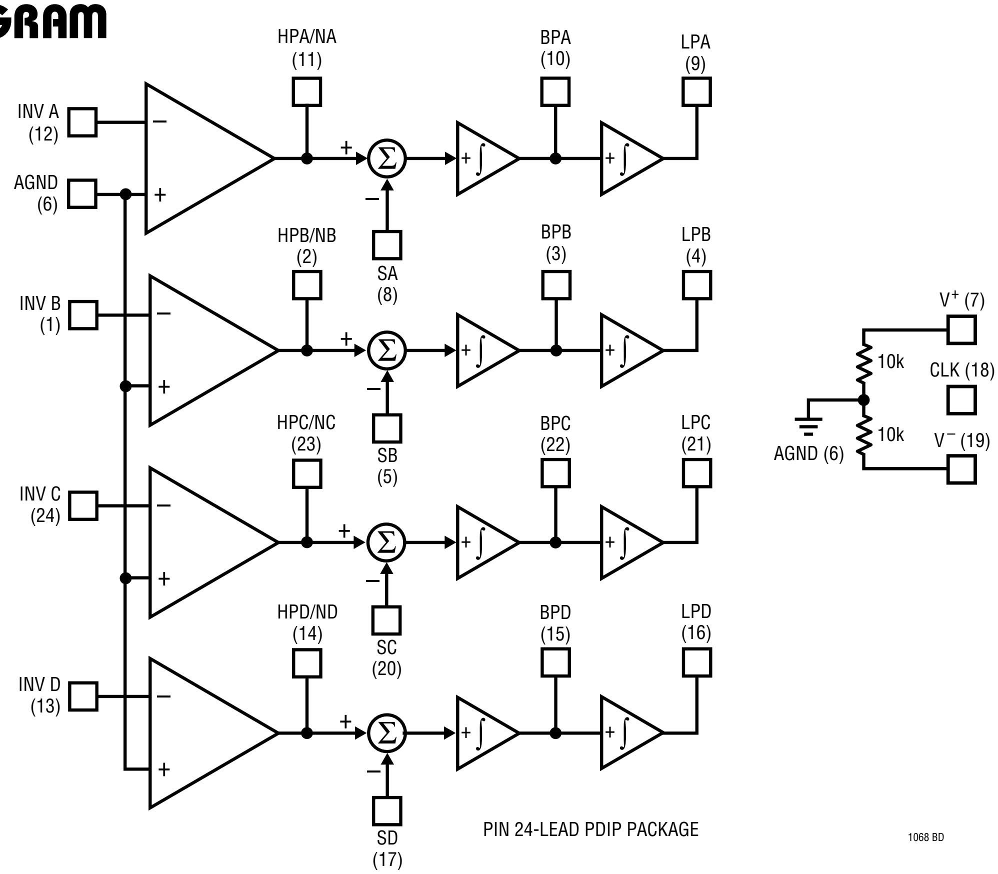
In a printed circuit layout any signal trace, clock source trace or power supply trace should be at least 0.1 inches away from any inverting input pins

Summing Input Pins

These are voltage input pins. If used, they should be driven with a source impedance below 5k. When they are not used, they should be tied to the analog ground pin.

The summing pin connections determine the circuit topology (mode) of each 2nd order section. Please refer to Modes of Operation.

BLOCK DIAGRAM



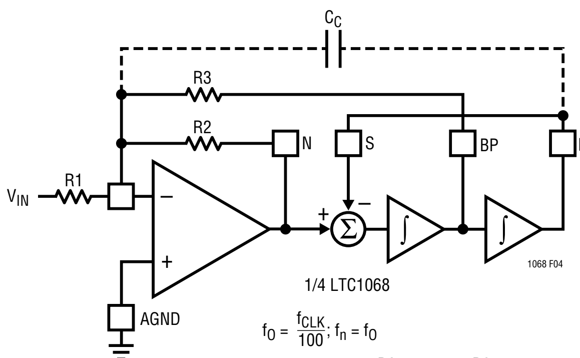
MODES OF OPERATION

For the definition of filter functions please refer to the LTC1060 data sheet.

Mode 1

In Mode 1, the ratio of the external clock frequency to the center frequency of each 2nd order section is internally fixed at 100:1. Figure 4 illustrates Mode 1 providing 2nd order notch, lowpass and bandpass outputs. Mode 1 can be used to make high order Butterworth lowpass filters; it can also be used to make low Q notches and for cascading 2nd order bandpass functions tuned at the same center frequency. Mode 1 is faster than Mode 3.

Please refer to the Operating Limits paragraph under Applications Information for a guide to the use of capacitor C_C.



$$f_O = \frac{f_{CLK}}{100}; f_n = f_O$$

$$Q = \frac{R3}{R2}; H_{ON} = -\frac{R2}{R1}; H_{OBP} = -\frac{R3}{R1}$$

$$H_{OLP} = H_{ON}$$

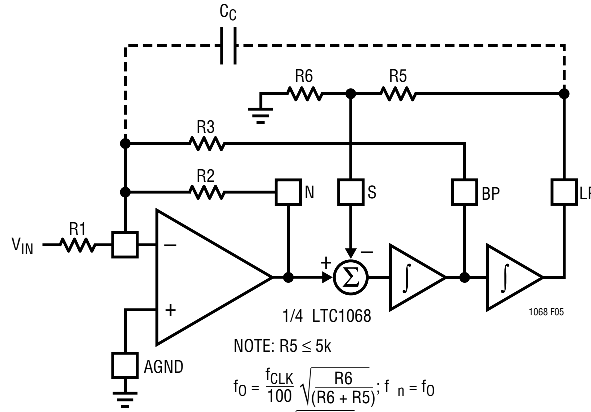
Figure 4. Mode 1, 2nd Order Filter Providing Notch, Bandpass and Lowpass Outputs

Mode 1b

Mode 1b is derived from Mode 1. In Mode 1b (Figure 5) two additional resistors R5 and R6 are added to lower the amount of voltage fed back from the lowpass output into the input of the SA (SB, SC or SD) switched-capacitor summer. This allows the filter's clock-to-center frequency ratio to be adjusted beyond 100:1. Mode 1b maintains the speed advantages of Mode 1 and should be considered an optimum mode for high Q designs with f_{CLK} to f_{CUTOFF} (or f_{CENTER}) ratios greater than 100:1.

The parallel combination of R5 and R6 should be kept below 5k.

Please refer to the Operating Limits paragraph under Applications Information for a guide to the use of capacitor C_C.



NOTE: R5 ≤ 5k

$$f_O = \frac{f_{CLK}}{100}\sqrt{\frac{R6}{(R6 + R5)}}; f_n = f_O$$

$$Q = \frac{R3}{R2}\sqrt{\frac{R6}{(R6 + R5)}}; H_{ON} = -\frac{R2}{R1}; H_{OBP} = -\frac{R3}{R1}$$

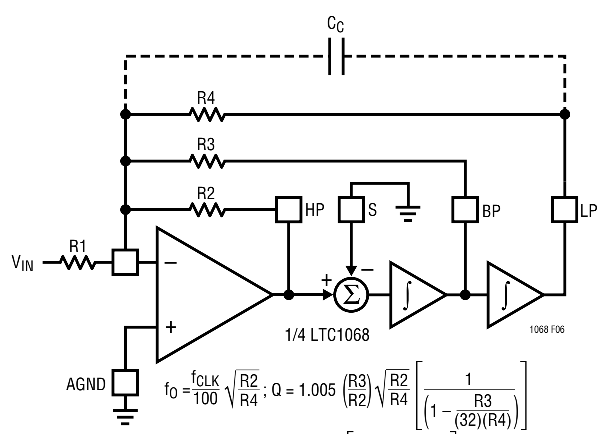
$$H_{OLP} = -\frac{R2}{R1}\left(\frac{R6 + R5}{R6}\right)$$

Figure 5. Mode 1b, 2nd Order Filter Providing Notch, Bandpass and Lowpass Outputs

Mode 3

In Mode 3, the ratio of the external clock frequency to the center frequency of each 2nd order section can be adjusted above or below 100:1. Figure 6 illustrates Mode 3, the classical state variable configuration, providing highpass, bandpass and lowpass 2nd order filter functions. Mode 3 is slower than Mode 1. Mode 3 can be used to make high order all-pole bandpass, lowpass and highpass filters.

Please refer to the Operating Limits paragraph under Applications Information for a guide to the use of capacitor C_C.



$$f_O = \frac{f_{CLK}}{100}\sqrt{\frac{R2}{R4}}; Q = 1.005\left(\frac{R3}{R2}\right)\sqrt{\frac{R2}{R4}}\left[\frac{1}{\left(1 - \frac{R3}{(32)(R4)}\right)}\right]$$

$$H_{OHP} = -\frac{R2}{R1}; H_{OBP} = -\frac{R3}{R1}\left[\frac{1}{\left(1 - \frac{R3}{(32)(R4)}\right)}\right]; H_{OLP} = -\frac{R4}{R1}$$

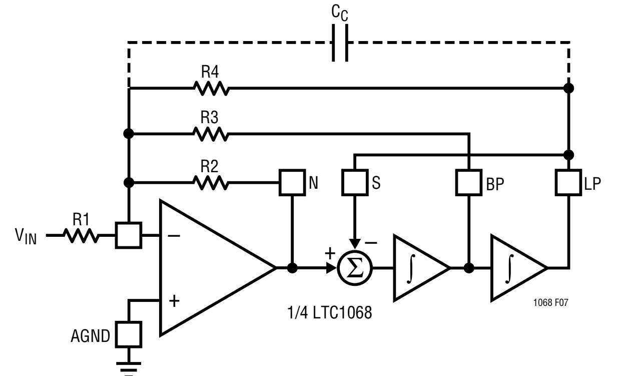
Figure 6. Mode 3, 2nd Order Section Providing Highpass, Bandpass and Lowpass Outputs

MODES OF OPERATION

Mode 2

Mode 2 is a combination of Mode 1 and Mode 3, shown in Figure 7. With Mode 2, the clock-to-center frequency ratio, f_{CLK}/f_O, is always less than 100:1. The advantage of Mode 2 is that it provides less sensitivity to resistor tolerances than does Mode 3. As in Mode 1, Mode 2 has a notch output that depends on the clock frequency and the notch frequency is therefore less than the center frequency, f_O.

Please refer to the Operating Limits paragraph under Applications Information for a guide to the use of capacitor C_C.



$$f_O = \frac{f_{CLK}}{100}\sqrt{1 + \frac{R2}{R4}}\ ;\ f_n = f_O$$

$$Q = 1.005\left(\frac{R3}{R2}\right)\sqrt{1 + \frac{R2}{R4}}\left[\frac{1}{\left(1 - \frac{R3}{(32)(R4)}\right)}\right]$$

$$H_{OHP} = -\frac{R2}{R1}\ (\text{AC GAIN, } f > f_n);\ H_{OHPn} = -\frac{R2}{R1}\left[\frac{1}{\left(1 + \frac{R2}{R4}\right)}\right](\text{DC GAIN, } f < f_n)$$

$$H_{OBP} = -\frac{R3}{R1}\left[\frac{1}{\left(1 - \frac{R3}{(32)(R4)}\right)}\right];\ H_{OLP} = H_{OHPn}$$

Figure 7. Mode 2, 2nd Order Filter Providing Highpass Notch, Bandpass and Lowpass Outputs

Mode 3a

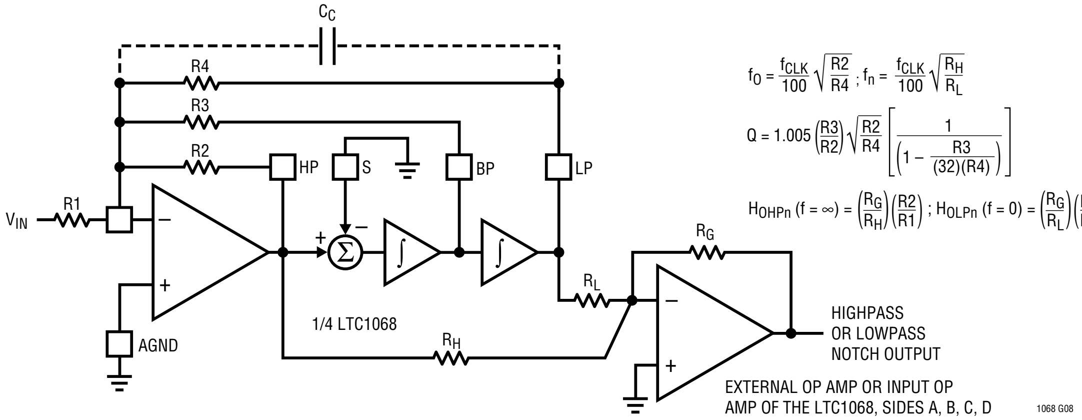
This is an extension of Mode 3 where the highpass and lowpass output are summed through two external resistors, R_H and R_L, to create a notch (see Figure 8). Mode 3a is more versatile than Mode 2 because the notch frequency can be higher or lower than the center frequency of the 2nd order section. The external op amp of Figure 8 is not always required. When cascading the sections of the LTC1068, the highpass and lowpass outputs can be summed directly into the inverting input of the next section.

Please refer to the Operating Limits paragraph under Applications Information for a guide to the use of capacitor C_C.

Mode 2n

This mode extends the circuit topology of Mode 3a to Mode 2 (Figure 9) where the highpass notch and lowpass outputs are summed through two external resistors, R_H and R_L, to create a lowpass output with a notch higher in frequency than the notch in Mode 2. This mode, shown in Figure 8, is most useful in lowpass elliptic designs. When cascading the sections of the LTC1068, the highpass notch and lowpass outputs can be summed directly into the inverting input of the next section.

Please refer to the Operating Limits paragraph under Applications Information for a guide to the use of capacitor C_C.



$$f_O = \frac{f_{CLK}}{100}\sqrt{\frac{R2}{R4}}\ ;\ f_n = \frac{f_{CLK}}{100}\sqrt{\frac{R_H}{R_L}}$$

$$Q = 1.005\left(\frac{R3}{R2}\right)\sqrt{\frac{R2}{R4}}\left[\frac{1}{\left(1 - \frac{R3}{(32)(R4)}\right)}\right]$$

$$H_{OHPn}(f = \infty) = \left(\frac{R_G}{R_H}\right)\left(\frac{R2}{R1}\right);\ H_{OLPn}(f = 0) = \left(\frac{R_G}{R_L}\right)\left(\frac{R4}{R1}\right)$$

Figure 8. Mode 3a, 2nd Order Filter Providing a Highpass Notch or Lowpass Notch Output

MODES OF OPERATION

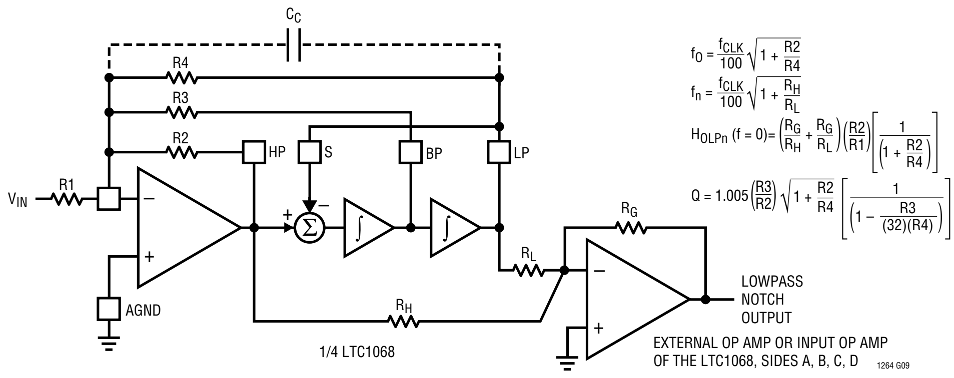


Figure 9. Mode 2n, 2nd Order Filter Providing a Lowpass Notch Output

APPLICATIONS INFORMATION

Operating Limits

The Maximum Q vs Frequency (f_O) graphs, under Typical Performance Characteristics, define an upper limit of operating Q for each LTC1068 2nd order section. These graphs indicate the power supply, f_O and Q value conditions under which a filter implemented with an LTC1068 will remain stable when operated at temperatures of 70°C or less. For a 2nd order section, a bandpass gain error of 3dB or less is arbitrarily defined as a condition for stability.

When the passband gain error begins to exceed 1dB, the use of capacitor C_C will reduce the gain error (capacitor C_C is connected from the lowpass node to the inverting node of a 2nd order section). Please refer to Figures 4 through 9. The value of C_C can be best determined experimentally, and as a guide it should be about 5pF for each 1dB of gain error and not to exceed 15pF. When operating the LTC1068 near the limits defined by the Typical Performance Characteristics graphs, passband gain variations of 2dB or more should be expected.

Clock Feedthrough

Clock feedthrough is defined as the RMS value of the clock frequency and its harmonics that are present at the filter's output pins. The clock feedthrough is tested with the filter's input grounded and depends on PC board layout and on the value of the power supplies. With proper layout techniques, the typical values of clock feedthrough are listed under Electrical Characteristics.

Any parasitic switching transients during the rising and falling edges of the incoming clock are not part of the clock feedthrough specifications. Switching transients have frequency contents much higher than the applied clock; their amplitude strongly depends on scope probing techniques as well as grounding and power supply bypassing. The clock feedthrough, can be greatly reduced by adding a simple RC lowpass network at the final filter output. This RC will completely eliminate any switching transients.

Wideband Noise

The wideband noise of the filter is the total RMS value of the device's noise spectral density and is used to determine the operating signal-to-noise ratio. Most of its frequency contents lie within the filter passband and cannot be reduced with post filtering. For a notch filter the noise of the filter is centered at the notch frequency.

The total wideband noise (μV_{RMS}) is nearly independent of the value of the clock. The clock feedthrough specifications are not part of the wideband noise.

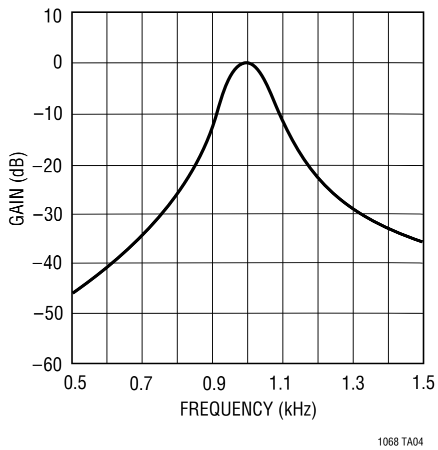
For a specific filter design, the total noise depends on the Q of each section and the cascade sequence.

Aliasing

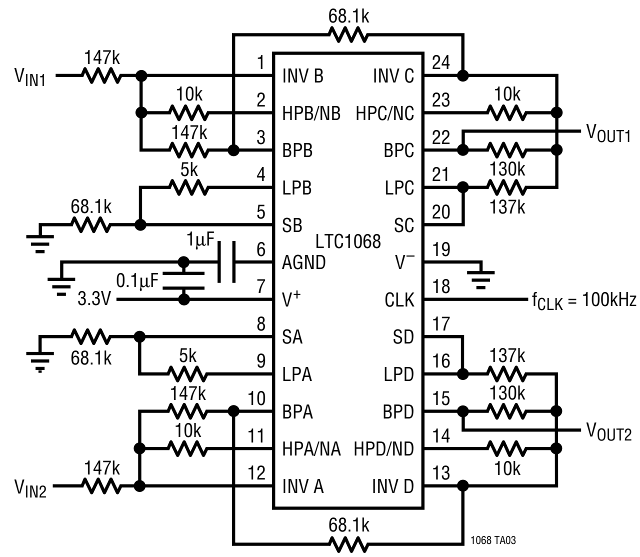
Aliasing is an inherent phenomenon of switched-capacitor filters and occurs when the frequency of the input signals that produce the strongest aliased components have a frequency, f_{IN}, such as ($f_{SAMPLING} - f_{IN}$) that falls into the filter's passband. For the LTC1068 the sampling frequency is twice f_{CLK}. If the input signal spectrum is not band-limited, aliasing may occur.

TYPICAL APPLICATIONS

Frequency Response



Single 3.3V Supply Dual Butterworth Bandpass Filter

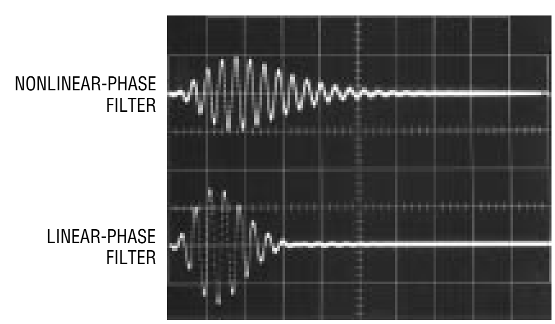


Linear Phase Bandpass Filters

The design of bandpass filters is very application specific; a great number of unique bandpass filters are possible. Linear phase bandpass filters are a special class of bandpass filters. Bandpass filters with linear phase response in their passband, feature an optimum transient response to an input signal of brief duration (for example, a short sinewave burst). The photo shows the transient responses of two bandpass filters with similar gain response and different passband phase response. Essentially, linear phase bandpass filters are used more for their signal selectivity than for their frequency selectivity. A linear phase bandpass filter can be a practical approximation to an ideal matched filter (a matched filter produces an optimum output signal-to-noise ratio in response to a specified, input signal). Two noteworthy applications of linear phase bandpass filters are the tone detection of short signal bursts and the processing of digital communication signals.

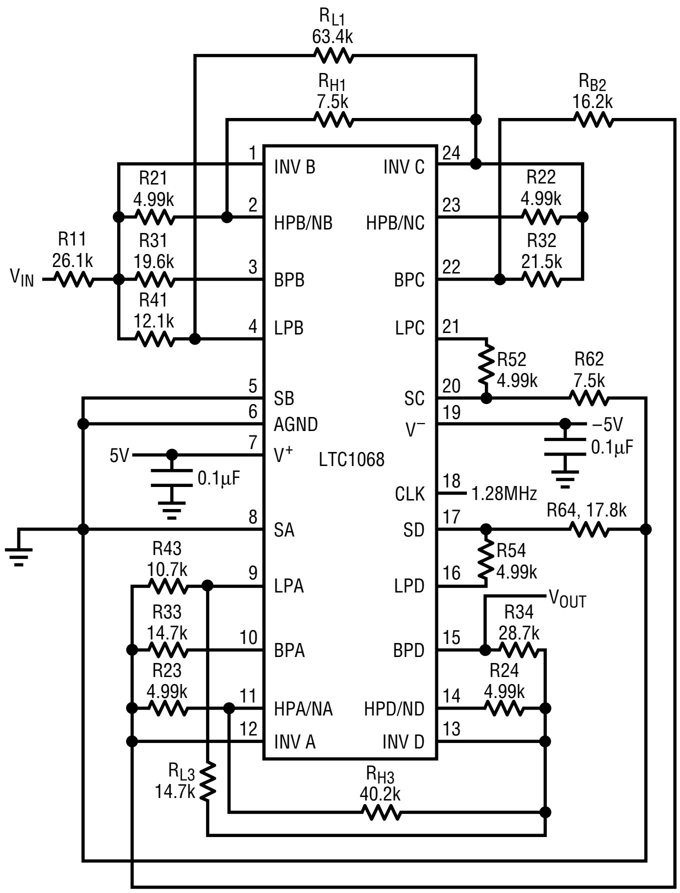
In digital communication systems, lowpass filters or bandpass filters are specified by a stopband attenuation roll-off factor. The roll-off factor is called the *alpha* of the filter and varies from zero to one. For practical filters, an *alpha* equal to one specifies a filter with at least 40dB attenuation at a frequency twice its –3dB frequency and an *alpha* equal to 1/2 specifies a filter with at least 40dB attenuation at 1 1/2 times it –3dB frequency. The following four filters are examples of linear phase bandpass filters. For comparison, each filter is shown with a center frequency of 10kHz; they can be clock tuned from 1Hz up to a center frequency determined by the maximum clock input, which depends on the filter's power supply.

Step Response



TYPICAL APPLICATIONS

Linear Phase Bandpass 8th Order 10kHz Filter



CENTER FREQUENCY (f_{CENTER}) = CLOCK FREQUENCY/128

PASSBAND –3dB BANDWIDTH = CENTER FREQUENCY/4.1
[LOWER $f_{–3dB}$ AT (0.88)(f_{CENTER}) AND UPPER $f_{–3dB}$ AT (1.12)(f_{CENTER})]

STOPBAND = –60dB AT (0.47)(f_{CENTER}) AND AT (2)(f_{CENTER})

MAXIMUM CLOCK FREQUENCY:
5MHz AT V_S = ±5V
2.7MHz AT V_S = 5V
800kHz AT V_S = 3.3V

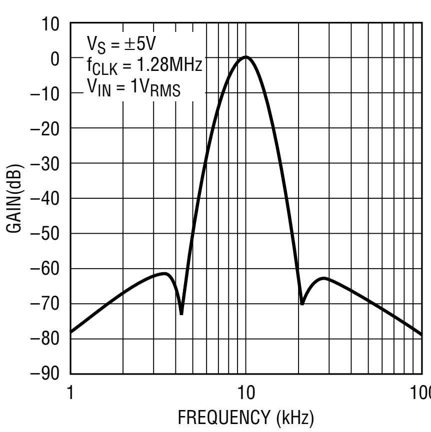
OUTPUT NOISE (FILTER INPUT AT GROUND) = 80µV_{RMS}

SPECIAL FEATURE: ALPHA = 0.6
[–40dB AT LOWER $f_{–3dB}$/1.6 AND UPPER ($f_{–3dB}$)(1.6)]

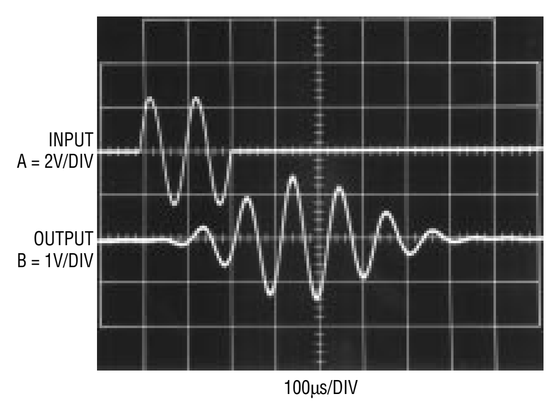
PINS 24-LEAD PDIP PACKAGE

LTC1068 • TA05a

Gain vs Frequency

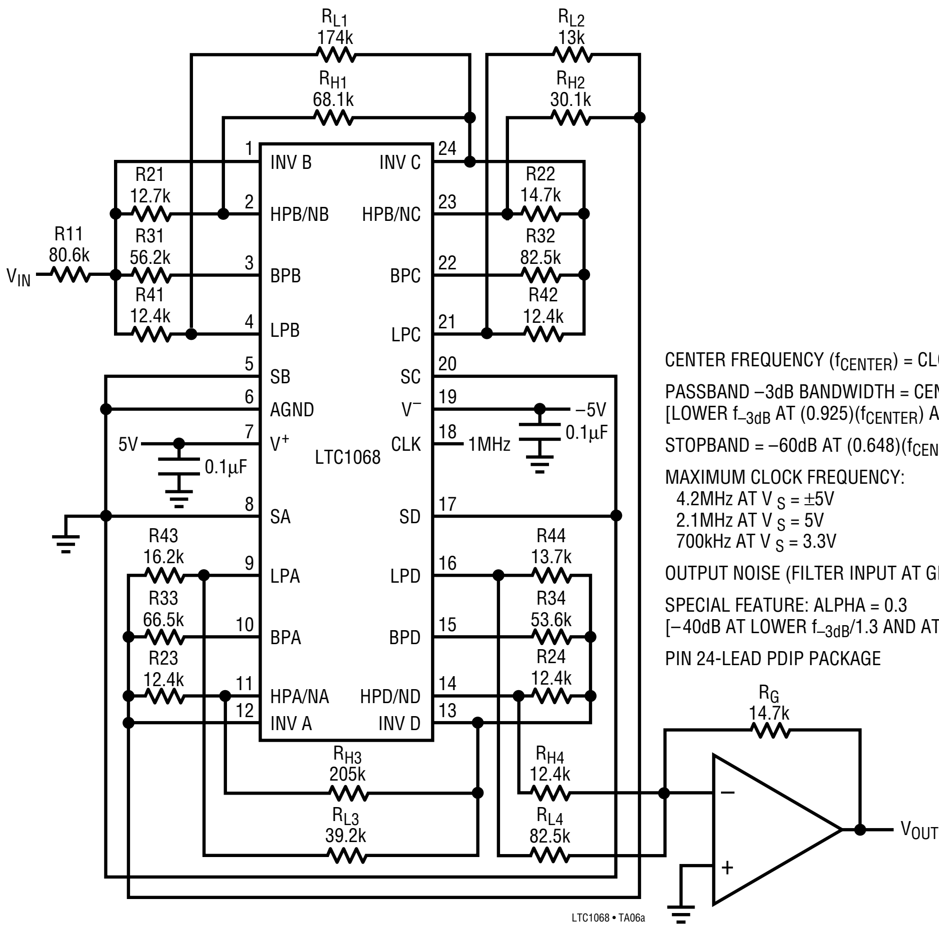


LTC1068 • TA05b



TYPICAL APPLICATIONS

Linear Phase Bandpass 8th Order 10kHz Filter



CENTER FREQUENCY (f_{CENTER}) = CLOCK FREQUENCY/100

PASSBAND –3dB BANDWIDTH = CENTER FREQUENCY/6.7
[LOWER $f_{–3dB}$ AT (0.925)(f_{CENTER}) AND UPPER $f_{–3dB}$ AT (1.075)(f_{CENTER})]

STOPBAND = –60dB AT (0.648)(f_{CENTER}) AND (1.475)(f_{CENTER})

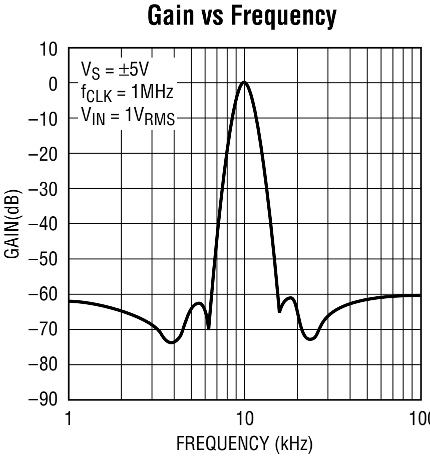
MAXIMUM CLOCK FREQUENCY:
4.2MHz AT V_S = ±5V
2.1MHz AT V_S = 5V
700kHz AT V_S = 3.3V

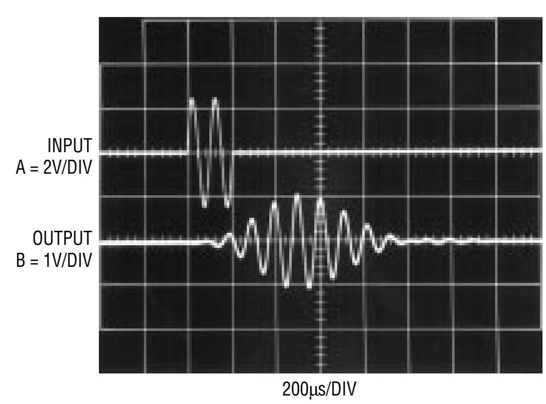
OUTPUT NOISE (FILTER INPUT AT GROUND) = 135µV_{RMS}

SPECIAL FEATURE: ALPHA = 0.3
[–40dB AT LOWER $f_{–3dB}$/1.3 AND AT UPPER ($f_{–3dB}$)(1.3)]

PIN 24-LEAD PDIP PACKAGE

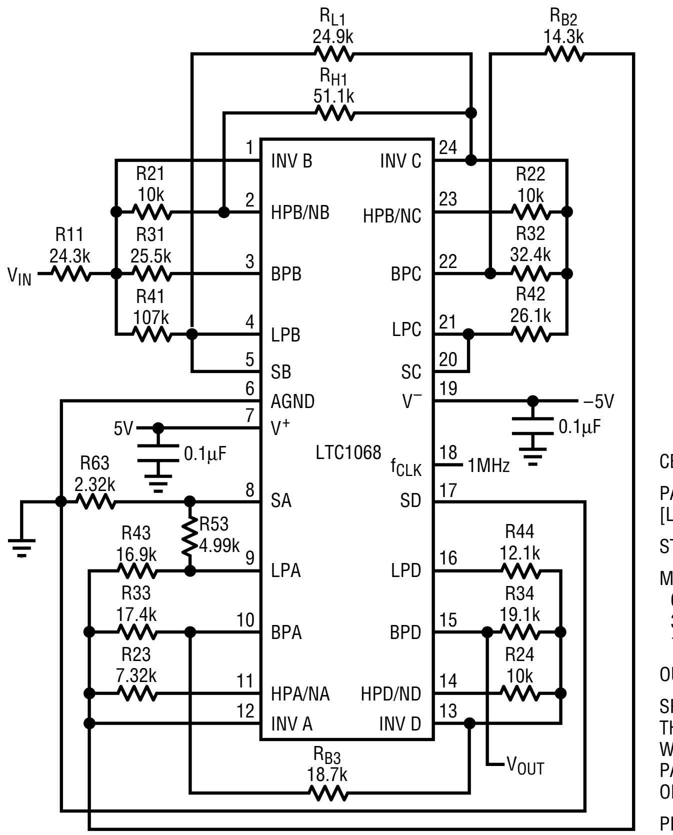
Gain vs Frequency





TYPICAL APPLICATIONS

Linear Phase Bandpass 8th Order 10kHz Filter



CENTER FREQUENCY (f_{CENTER}) = CLOCK FREQUENCY/100

PASSBAND –3dB BANDWIDTH = CENTER FREQUENCY/4.1
[LOWER f_{-3dB} AT (0.88)(f_{CENTER}) AND UPPER f_{-3dB} AT (1.12)(f_{CENTER})]

STOPBAND = –50dB AT (0.3)(f_{CENTER}) AND AT (1.65)(f_{CENTER})

MAXIMUM CLOCK FREQUENCY:
6MHz AT V_S = ±5V
3MHz AT V_S = 5V
1MHz AT V_S = 3.3V

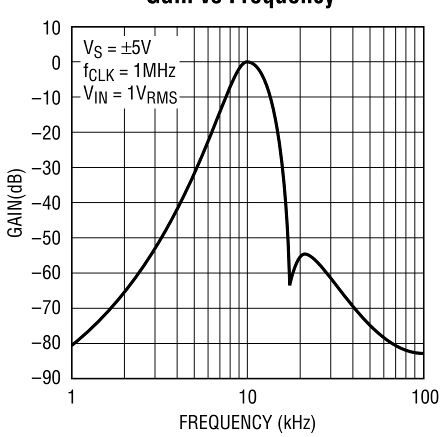
OUTPUT NOISE (FILTER INPUT AT GROUND) = 65µV_{RMS}

SPECIAL FEATURE: HIGH SELECTIVITY IN UPPER STOPBAND. THIS BANDPASS FILTER CAN REJECT A STRONG NOISE SIGNAL WHOSE FREQUENCY IS NEAR A WEAK SIGNAL IN THE FILTER'S PASSBAND. EXAMPLE; DETECTING A 10kHz TONE IN THE PRESENCE OF A 15.74kHz NOISE

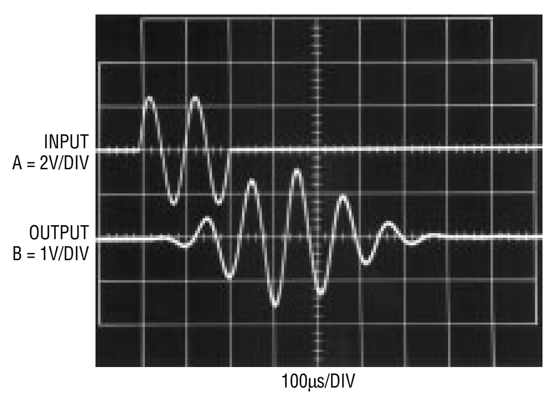
PIN 24-LEAD PDIP PACKAGE

LTC1068 • TA07a

Gain vs Frequency

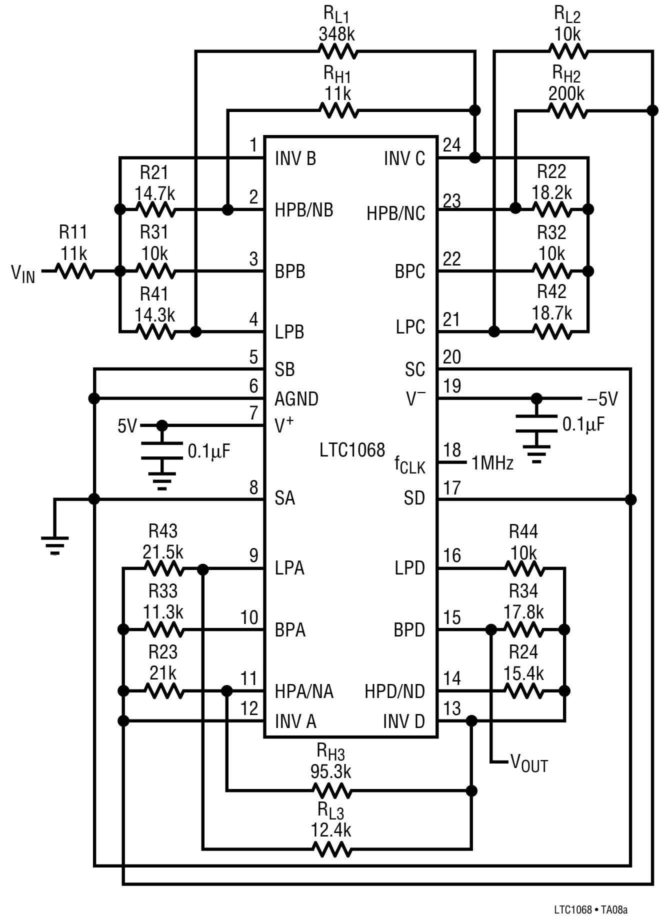


LTC1068 • TA07b



TYPICAL APPLICATIONS

Linear Phase Bandpass 8th Order 10kHz Filter



CENTER FREQUENCY (f_{CENTER}) = CLOCK FREQUENCY/100

PASSBAND –3dB BANDWIDTH = CENTER FREQUENCY/1.67
[LOWER f_{-3dB} AT (0.7)(f_{CENTER}) AND UPPER f_{-3dB} AT (1.3)(f_{CENTER})]

STOPBAND = –42dB AT (0.2)(f_{CENTER}) AND AT (2.5)(f_{CENTER})

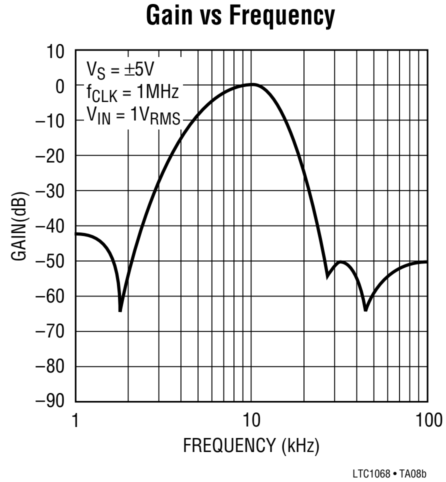
MAXIMUM CLOCK FREQUENCY:
6MHz AT V_S = ±5V
3MHz AT V_S = 5V
1MHz AT V_S = 3.3V

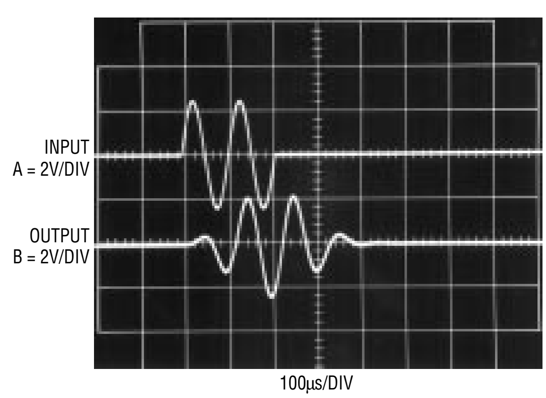
OUTPUT NOISE (FILTER INPUT AT GROUND) = 45µV_{RMS}

SPECIAL FEATURE: WIDEBAND BANDPASS FILTER WITH EXCELLENT TRANSIENT RESPONSE. THE FILTER'S OUTPUT IN RESPONSE TO A SINUSOIDAL PULSE IS ALMOST A MIRROR IMAGE OF ITS INPUT

PIN 24-LEAD PDIP PACKAGE

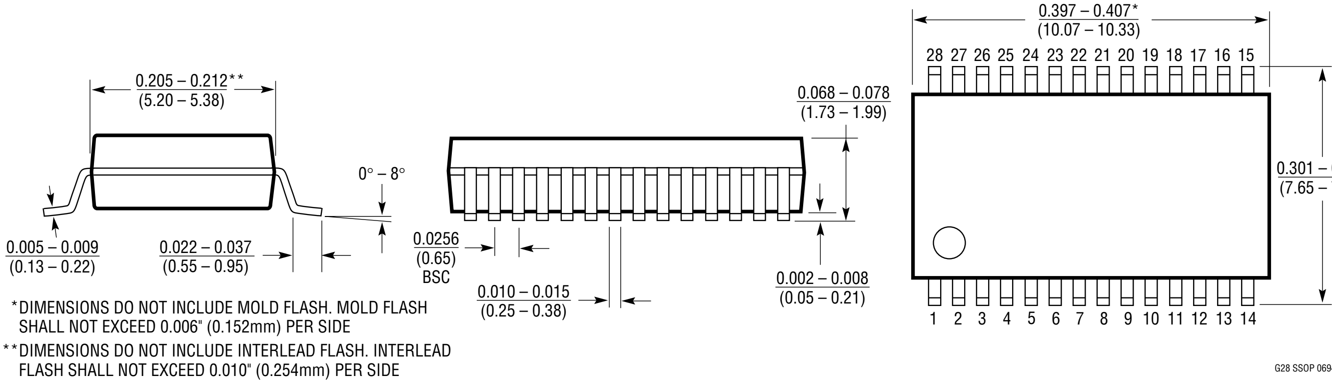
Gain vs Frequency





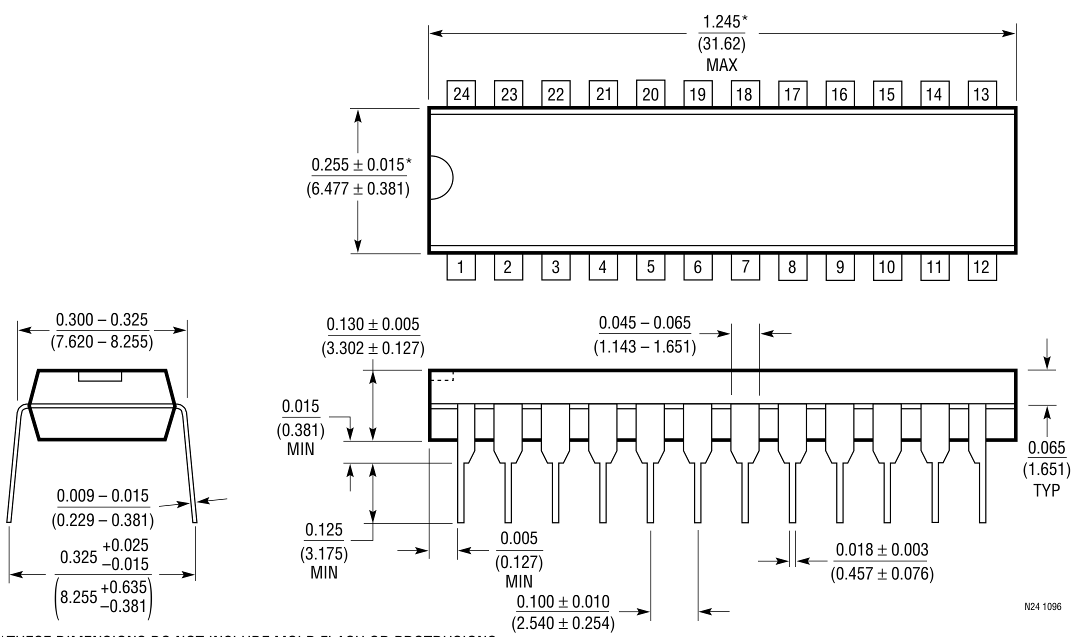
PACKAGE DESCRIPTION **Dimensions in inches (millimeters) unless otherwise noted.**

G Package
28-Lead Plastic SSOP (0.209)
(LTC DWG # 05-08-1640)



*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE
**DIMENSIONS DO NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

N Package
24-Lead PDIP (Narrow 0.300)
(LTC DWG # 05-08-1510)



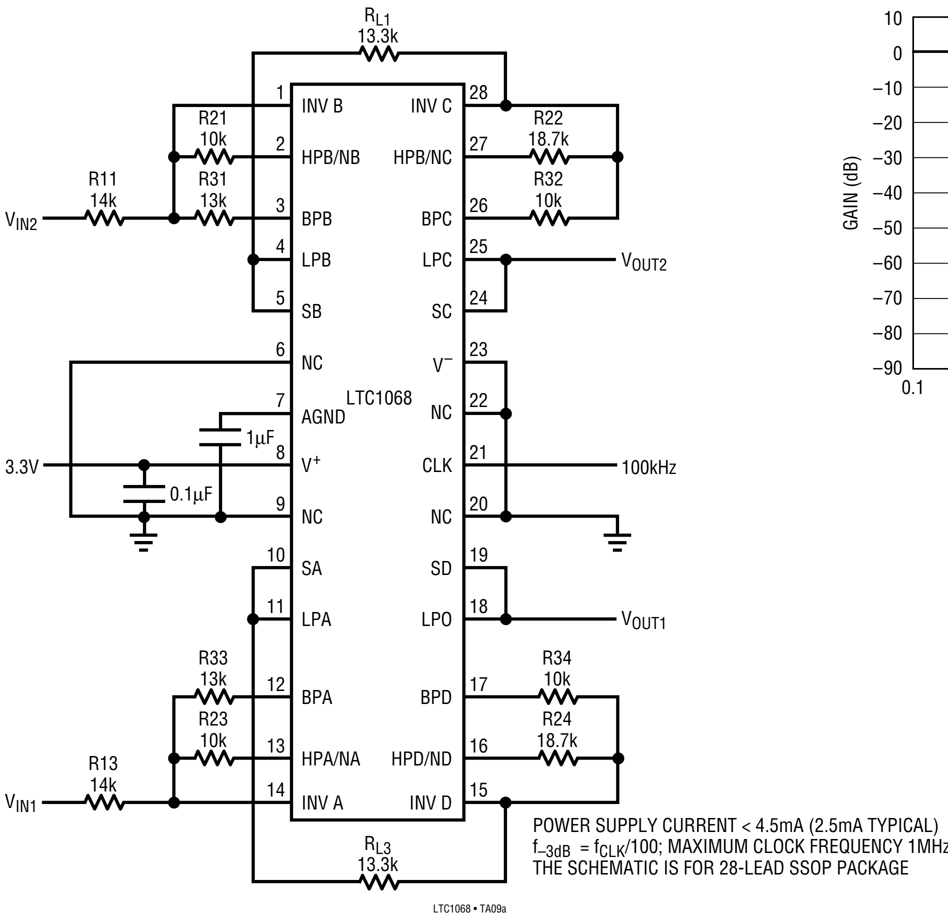
*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.010 INCH (0.254mm)

LINEAR TECHNOLOGY

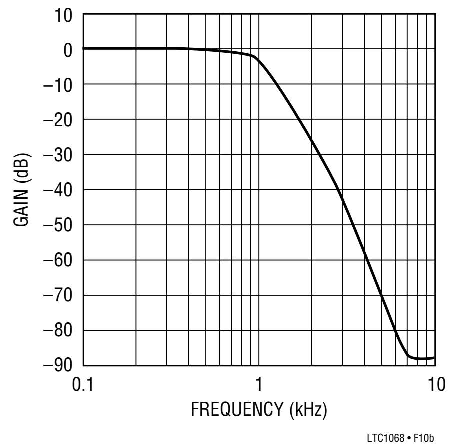
Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

TYPICAL APPLICATION

Single 3.3V Supply, Low Power, Dual Butterworth Lowpass Filters



Dual 4th Order Butterworth Gain vs Frequency



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1064	Universal Filter	50:1 and 100:1 Clock-to-f_0 Ratios
LTC1164	Low Power Universal Filter	50:1 and 100:1 Clock-to-f_0 Ratios
LTC1264	High Speed Universal Filter	20:1 Clock-to-f_0 Ratio

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